Nature of Interface Defect Buildup in Gated Bipolar Devices Under Low Dose Rate Irradiation

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***Abstract*—The buildup of radiation-induced switching states in ELDRS-sensitive bipolar base oxides is measured with dc current-voltage and charge pumping techniques. These states include both faster interface traps (P_b centers) and slower border traps. After irradiation, border traps and interface traps mostly decrease with annealing time and temperature in devices irradiated at 0 V. However, for devices irradiated at −50 V, there is a decrease in border trap density but an increase in interface trap density. These differences in interface-trap buildup and annealing are attributed to the dependence of defect passivation and depassivation on the concentrations of hydrogen and dangling Si bond defects near the Si/SiO_2 interface.**

***Index Terms*—Bipolar junction transistors, border traps, charge pumping, ELDRS, interface traps.**

I. Introduction

THE operation of bipolar junction transistors is affected strongly by radiation-induced switching state (N_{ss}) build-up in bipolar base oxides [1]–[4]. These states increase surface recombination, which in turn leads to an increase in base current and dc current gain degradation [1]–[4]. The primary goal of this work is to identify the physical nature of radiation-induced switching states by examining the rate at which these states exchange charge with the underlying silicon. There are primarily two types of switching states: 1) interface traps, which are dangling Si bonds (P_b centers) at the Si/SiO_2 interface as illustrated in Figs. 1 and 2) border traps [5]–[7].

Interface traps are formed when hydrogen ions (H^+), released by the generation of electron-hole pairs due to ionizing radiation exposure and the subsequent charge transport [9], migrate to a Si-SiO_2 interface and react with Si-H bonds. The reaction between H^+ and the Si-H complexes releases H_2, creating interface traps [10]. In this paper we will denote interface trap density as N_{it}. Under positive bias, H^+ release in the oxide typically dominates the interface-trap formation [9]. However, recent experiments suggest that proton release in the oxide bulk may not be the only cause of interface trap formation [11], [12]. Most notably, this model cannot easily account for significant interface trap buildup under negative gate bias [11], [12], since the transport of H^+ in the oxide to the interface is greatly reduced in this case. Interface-trap buildup under negative bias has been attributed to proton release from dopant complexes in the Si [13].

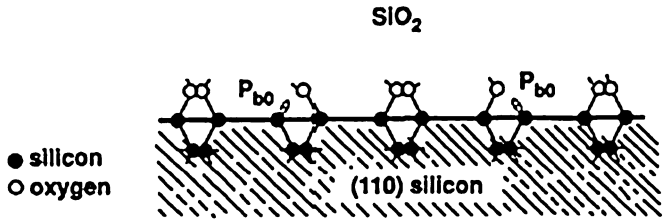

Fig. 1. Schematic illustration of P_b center interface trap defects [8].

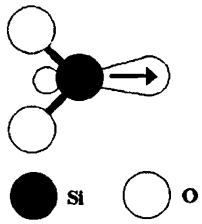

Fig. 2. Schematic illustration of E' center in SiO_2[14].

Border traps are E' center oxygen defects (trivalent Si centers in SiO_2 associated with oxygen vacancies) near the Si/SiO_2 interface, illustrated in Fig. 2. Like interface traps, border traps are also created by radiation exposure, and the buildup can be a strong function of gate bias [15]. However, once created, the rate at which charge is exchanged with border traps typically is much slower compared to interface traps [16], [17]. We will denote border trap density as N_{bt}.

The potential for having both border traps and interface traps suggests that the total density of switching states at the interface is:

$$N_{ss} = N_{it} + N_{bt}. \tag{1}$$

Through the use of DC characterization and charge pumping experiments, concentrations of N_{it} and N_{bt} can be estimated independently.

In this paper, we investigate the formation and annealing of switching states during biased low dose rate and subsequent annealing experiments as a function of electric field and tempera-

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ture during exposure. These results provide further insight into radiation induced interface defect formation in bipolar devices.

II. Experimental Results

A. Pre-Anneal Results

The Gated Lateral PNP (GLPNP) bipolar transistors analyzed in this work were designed at NAVSEA Crane and manufactured in National Semiconductor Corporation's standard bipolar linear IC process flow in Arlington, Texas. The devices have an independent metal gate electrode that covers the base region of the transistor, allowing independent control of the surface potential. They are part of a process lot fabricated with six unique passivation splits that was designed to enable the isolation of mechanisms for ELDRS in bipolar parts. The GLPNP transistors examined in this work were fabricated with P-glass passivation. The oxide thickness and gate area of the device are $\sim$1.2 μm and $\sim$1440 μm^2, respectively. The low-dose-rate (LDR) experiment was performed at the gamma radiation facility on the campus of the University of Arizona. The devices under test were irradiated at approximately 49 mrad(SiO_2)/s for 56.7 h to 10 krad(SiO_2) at gate biases of 0 V and -50 V. The devices were not irradiated at positive bias because previous work shows no ELDRS effects in these devices for these conditions [11]. Immediately following the exposure, device current-voltage (I-V) characteristics were obtained with the gate sweep and sub-threshold sweep techniques described below. Radiation induced interface defect buildup was also estimated through charge pumping experiments. For the base current versus gate voltage (gate sweep or GS) measurements, the base current was monitored with a HP4156 parameter analyzer while the gate was swept in 1 V steps from accumulation to inversion (80 V to -100 V). During the GS tests, the GLPNP transistors were biased in the forward active mode during measurement as the gate voltage was varied, with collector, base, and substrate grounded and the emitter voltage fixed at 0.5 V. For the sub-threshold I-V measurements, the gate was swept from 10 V to -100 V in 1 V steps; the emitter was biased at -0.1 V and collector and base were grounded.

Fig. 3 is a plot of I_b versus V_g curves for 0 V and -50 V biased devices immediately after irradiation. Each curve represents the average GS data taken from all devices irradiated with identical bias conditions. These results are similar to data reported in [11]. Here the I_b versus V_g curves for 0 V and -50 V irradiation biases differ in several respects. First, the peak base current amplitude for 0 V biased devices is greater than for the -50 V biased devices. Second, the curve has a much greater shift in the negative voltage direction in the -50 V devices, while there is hardly any shift to the left for the 0 V devices compared to the pre-irradiation response. Positive oxide trapped charge (N_{ot}) has been shown to cause the horizontal shift in the base current curve, and switching states (N_{ss}) can increase the base current amplitude [16]. Therefore, the results in Fig. 3 indicate that N_{SS} is greater in the devices irradiated at 0 V than those irradiated at -50 V, and N_{ot} is greater in the devices biased at -50 V. Curves from the subthreshold sweep in Fig. 4 show similar results. The horizontal shift of the subthreshold current curves indicates N_{ot} buildup and the change

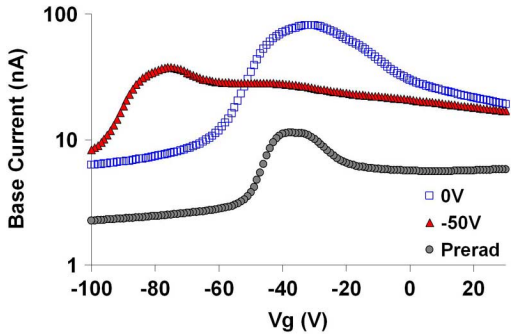

Fig. 3. Average Gate Sweep response of post-irradiation GLPNP devices under 0 V and -50 V irradiation biases.

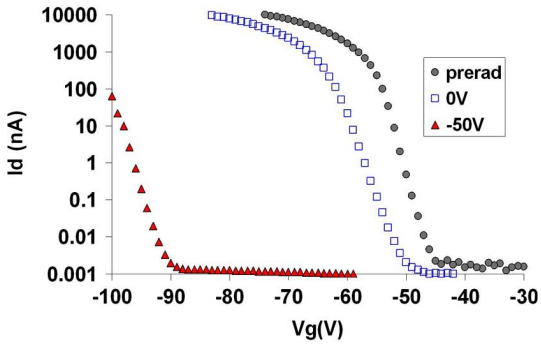

Fig. 4. Average subthreshold response of post-irradiation GLPNP devices under 0 V and -50 V irradiation biases.

in sub-threshold slope signifies that switching states are created during irradiation.

To help distinguish the effects of (faster) interface and (slower) border traps, we performed charge pumping (CP) experiments on these devices [16], [17]. By charge pumping the gate at different frequencies, we can separate border traps from interface traps [16]. At high frequencies, the charge recombined per cycle mostly detects fast switching states, i.e., interface traps [16], [18]. This is true because border traps do not have enough time to exchange charge with the underlying semiconductor. At much lower frequencies, on the order of 10 to 100 Hz, the probability of charge exchange with border traps increases, and at least a fraction of these defects can then be effectively probed [17].

Fig. 5 shows the charge recombined per cycle versus pulse frequency from the frequency-dependent charge pumping experiments for devices irradiated at both 0 V and -50 V bias. Fig. 5 shows that the devices irradiated at -50 V exhibit increased charge recombined per cycle as the frequency is decreased from 1000 Hz to 50 Hz. This response is a signature of border traps [16]. In the 0 V biased devices, the charge recombined per cycle decreases with reduced frequency. Since these data do not exhibit an increase in recombined charge at low frequencies, we conclude that fewer border traps are generated at 0 V bias. The characteristic decrease in recombined charge per unit cycle with decreasing frequency is caused by a combination of: a) trap emission and carrier collection at the source and drain due to different fall and rise times of the charge pumping pulse at different frequencies, and b) recombination in bulk defects

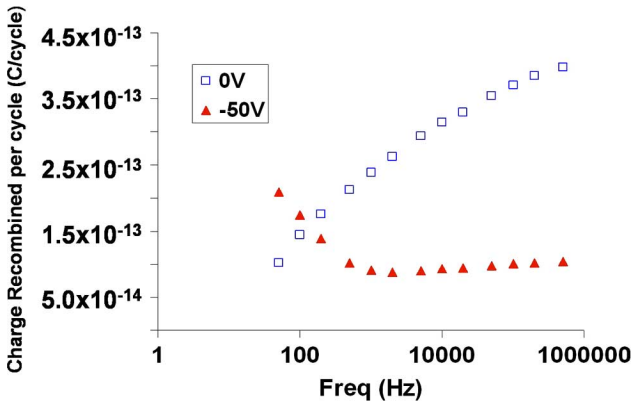

Fig. 5. Average charge recombined per cycle versus frequency for devices with -50 V and 0 V irradiation biases. The figure indicates a much higher density of N_{it} in the 0V biased parts and higher N_{bt} in the -50 V parts.

TABLE I
ESTIMATED N_{it} FROM FREQUENCY CP AFTER ANNEALING

	0V	-50V
N_{it} (cm^{-2})	~ $3x10^{11}$	~ $9x10^{10}$
N_{bt} (cm^{-2})	N/A	~ $9x10^{10}$

associated with the geometric contribution to charge pumping [19], [20]. Each of these terms acts to reduce the recombined charge per unit cycle, in contrast to the contributions of border traps, which increase this charge. Thus, the curves in Fig. 5 relate to a lower bound of the interface and border trap densities. Nevertheless, Fig. 5 clearly indicates differences in interface and border trap densities in the devices irradiated at 0 V and -50 V.

From the charge recombined per cycle versus frequency data, we can estimate the average interface trap density, N_{it}, with the following equation [19]:

$$N_{it} = \frac{\partial Q_{ss}}{\partial \log(f)} \frac{\log(e)}{2qkTA_G} E_{BG}, \tag{2}$$

where Q_{ss} is the charge recombined per cycle, E_{BG} is the Si band gap, and A_G is the area under the gate. We can also estimate border trap density by computing the slope of the curve at lower frequencies [21]:

$$N_{bt}(x_m) \approx -\frac{dQ_{ss}}{dlogf} \frac{\alpha_{ox}}{2.3qA_G}, \tag{3}$$

where α_{ox} is the carrier attenuation coefficient in SiO_2[22]. Here $N_{bt}X_m$ is in units of cm^{-3} and is a function of the maximum tunneling distance associated with the measurement frequency [21]. To approximate the N_{bt} areal density, we simply multiply $N_{bt}(X_m$ by its maximum tunneling distance x_m for the lowest frequency data point. The value of N_{bt} obtained here is an upper bound of border trap densities

$$N_{bt} \approx N_{bt}(x_m)\mathbf{x}_m. \tag{4}$$

Table I lists the estimated interface trap and border trap areal densities obtained from the above equations.

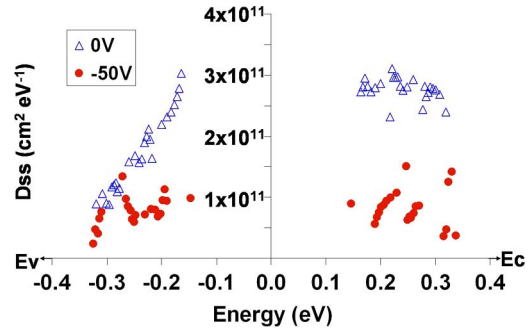

Fig. 6. Average N_{ss} energy distribution for devices irradiated with -50 V and 0 V biases.

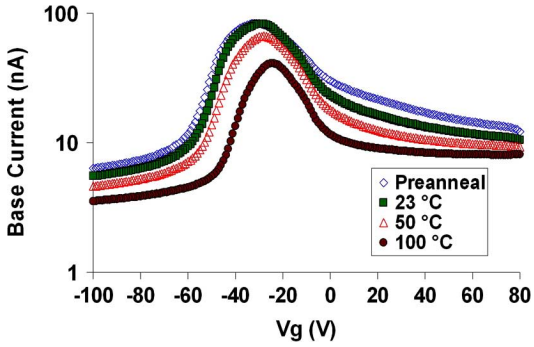

Fig. 7. Average gate sweep results after three different temperature anneals among devices with 0 V irradiation biases.

Using the trapezoidal pulse method, the switching state energy distribution (D_{ss} (E)) was calculated for both 0 V and -50 V irradiated devices. Since trapezoidal CP uses the rise and fall times of the pulse to determine the energy location of the interface states, there is sufficient time for border traps to exchange charge with the silicon if the rise and fall times are long enough. The slow rise and fall times used here correspond to energy levels close to midgap [19], so the inferred switching state density at these energy levels can be a combination of interface traps and border traps. Fig. 6 shows the D_{ss} versus energy plots for both 0 V and -50 V devices. The energy distribution data for devices with radiation biases of 0 V and -50 V are also distinctly different here. Similar to the frequency-dependent CP results, the average switching state density for the 0 V biased devices is larger than for the -50 V devices. The inferred trap densities estimated from trapezoidal CP matches well the extracted values in Table I As Fig. 6 indicates, in the 0 V biased device, an asymmetric distribution of N_{ss} above and below midgap is observed, which is similar to the results obtained from the same devices irradiated at high dose rates, i.e., N_{ss} density above midgap is greater than that below mid-gap [23]. However, the N_{ss} distribution is fairly symmetric for devices irradiated at -50 V.

B. Annealing Results

Post irradiation annealing was performed on the devices for three different temperatures: 23°C, 50°C, and 100°C. All devices were annealed for a period of 7 days in temperature chambers at Arizona State University. During post-irradiation annealing, all terminals were grounded. Fig. 7 shows the gate

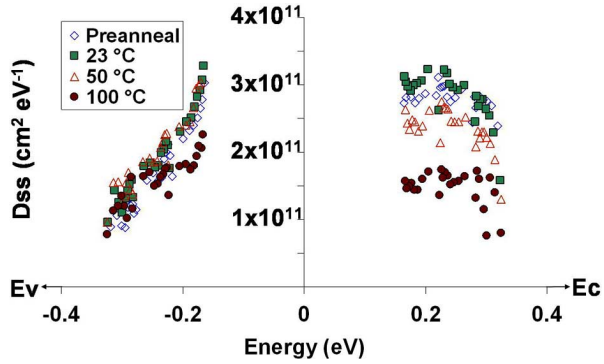

Fig. 8. Average N_{ss} energy distribution after annealing for devices with 0 V irradiation biases.

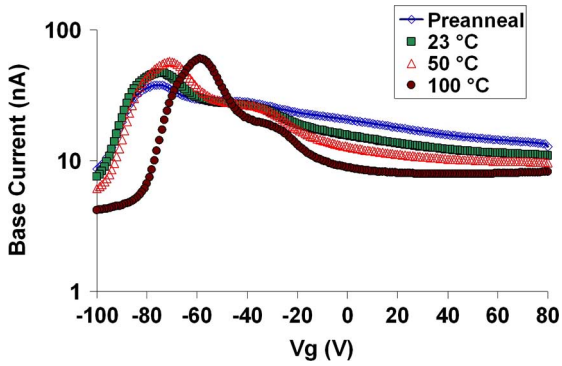

Fig. 10. Average gate sweep results after three different temperature anneals among devices with -50 V irradiation biases.

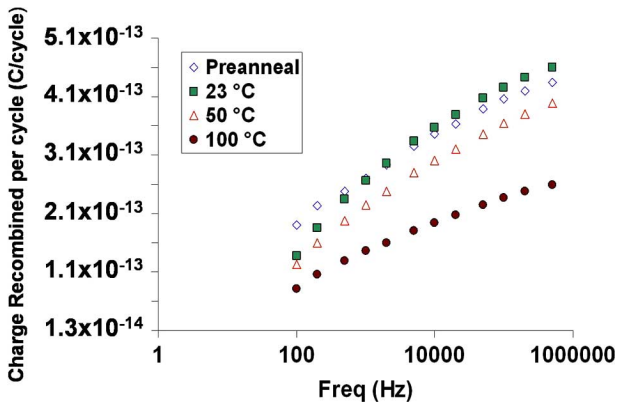

Fig. 9. Average charge recombined per cycle versus frequency for devices with 0 V irradiation biases after post-irradiation annealing. The figure indicates annealing of interface traps and no evidence of high border trap density in these devices.

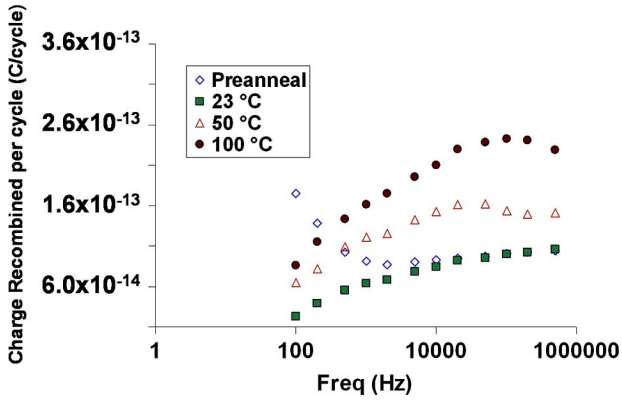

Fig. 11. Average charge recombined per cycle versus frequency for devices with -50 V irradiation biases after post-irradiation annealing. The figure indicates enhancement of interface traps and annealing of border traps in these devices.

TABLE II
ESTIMATED N_{it} FROM FREQUENCY CP

0V devices	N_{it}	N_{bt}
Preanneal	~ 3x10¹¹	N/A
23 °C	~ 3.3x10¹¹	N/A
50 °C	~ 2.8x10¹¹	N/A
100 °C	~ 1.9x10¹¹	N/A

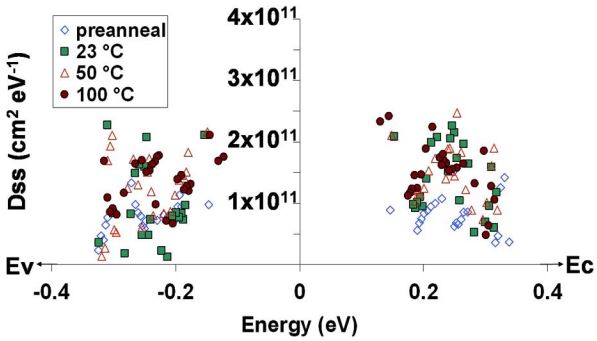

Fig. 12. Average N_{ss} energy distribution after annealing for devices with -50 V irradiation biases.

sweep results for devices irradiated under 0 V gate bias and annealed at the three different temperatures.

The decrease in base current width and peak amplitude in Fig. 7 shows annealing of switching states at 50°C and 100°C for the 0 V biased devices. Using the trapezoidal charge pumping technique, the energy distribution of interface states is measured and plotted in Fig. 8. These results confirm the annealing of N_{ss} at 50°C and 100°C. Frequency-dependent charge pumping is used again to separate the two defect types in Fig. 9. There is no evidence of a significant concentration of border traps in these devices, and there is a strong temperature-dependent annealing of interface traps. The extracted interface trap densities after annealing from the frequency CP are shown in Table II.

The corresponding annealing results for -50 V irradiation-biased devices are shown in Figs. 10–12. Fig. 10 shows the gate sweep results. From the amplitude of the current peaks, the data suggest a small increase in switching state density after annealing at various temperatures. The shift of the current profile to the right suggests annealing of oxide trapped charge.

Fig. 11 and Table III show the frequency-dependent CP results from the same devices. These data confirm an increase of interface trap densities during annealing, and indicates the removal of a majority of the border traps, since the charge recombined per cycle drops dramatically at lower frequencies.

The switching state energy distribution from trapezoidal CP in Fig. 12 is consistent with a combination of an increase in

TABLE III
ESTIMATED N_{it} FROM FREQUENCY CP AFTER ANNEALING

-50V devices	N_{it}	N_{bt}
Preanneal	~ $9x10^{10}$	~$9x10^{10}$
23 °C	~ $9x10^{10}$	N/A
50 °C	~ $1.3x10^{11}$	N/A
100 °C	~ $1.7x10^{11}$	N/A

interface-trap density and a decrease in border-trap density, leading to only a small change in the total density of switching states.

III. DISCUSSION

In previous work both Pease *et al.* and Shaneyfelt *et al.* showed a significant amount of annealing of switching states (possibly a combination of interface traps and border traps) at $100°C$[11], [12]. Moreover, in MOS devices, N_{it} annealing typically is not observed for temperatures below 100°C [24], though some annealing of N_{it} has been reported in MOSFETs at these temperatures for high amounts of damage and low electric fields [25]. In our experiments, for 0 V biased devices, the annealing results at $50°C$ and $100°C$are consistent with [11], [12].

It is interesting that interface trap densities decrease with increasing annealing time and temperature for devices irradiated with 0 V bias Table II, but increase for the same annealing sequences for devices irradiated at -50 V bias. This difference in annealing response is caused primarily by the differences in defect densities after irradiation for the two cases, in conjuction with the high hydrogen concentrations in these devices [11], [12], [26]. The initial interface trap density after irradiation is larger after irradiation for the 0 V bias case than the -50 V bias case. For a relatively higher initial defect density, the passivation of dangling bonds at the Si/SiO_2 interface can dominate over the creation of new interface traps [26], [27]. For lower initial densities, interface-trap buildup tends to dominate [26].

The frequency charge pumping results show no significant border trap formation and annealing in the 0V irradiation-biased devices. Hence, the observed annealing of switching states in the 0 V devices is predominately due to the annealing of interface traps. The results for the 0 V annealing data are qualitatively consistent with the model described in [26] and the data of [28]. In these cases, the behavior of the post-irradiation interface-trap density depends on the annealing temperature; i.e., at higher annealing temperatures, N_{it} decreases with time, and at lower temperatures, N_{it} increases with time. These results confirm that interface-trap annealing can occur in bipolar devices at lower temperatures than is typically observed in MOS devices. This is mostly likely due to the high defect concentrations and hydrogen densities in these devices [11], [12], [26]. Consistent with work in [28], differences in interface-trap and border-trap annealing as a function of temperature are also observed in these devices. This work shows the importance of separating these two effects to understand fully linear bipolar radiation response.

The GLPNP devices used in this study were fabricated in the same bipolar process as other commercial linear bipolar devices. The gate of the GLPNP device is used to independently control the surface potential in the device to study device level effects of radiation. The range of surface potential accessed by this test structure includes the surface potential that would occur in a bipolar device without the gate terminal. Therefore, the nature of radiation induced defects and post-irradiation behavior in the GLPNP devices discussed here can be directly applied to other commercial bipolar devices fabricated in the same process.

IV. CONCLUSION

In this paper, the nature of radiation induced switching state buildup in ELDRS-sensitive bipolar devices is investigated via low-dose-rate irradiation as a function of bias and post-irradiation annealing temperature. Both interface and border traps are observed to contribute significantly to the radiation-induced damage in linear bipolar devices. For devices irradiated under 0 V bias, the switching states are shown to be primarily interface traps. For devices with -50 V irradiation bias, a combination of interface traps and border traps is found. Post-irradiation annealing shows removal of interface traps for 0 V irradiated devices at temperatures below 100°C. In -50 V irradiated devices,post-irradiation annealing of border traps and an increase in interface trap density were observed. These results confirm the importance of both interface and border traps to the radiation response of linear bipolar transistors, and demonstrate that the respective annealing responses of these defects can differ significantly.

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